Introduction to Megafunctions

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Overview

With programmable logic device (PLD) densities reaching 250,000 gates, it is now possible to implement entire digital subsystems on a single PLD. However, designing at higher density levels poses a new set of challenges. Creating state-of-the art circuitry while meeting the demand of shrinking development cycles requires a new design approach.

Altera addresses this design need with Altera-created megafunctions, called MegaCore™ functions, and megafunctions developed through the Altera Megafunction Partners Program (AMPP℠). Megafunctions are ready-made, pre-tested functional blocks that augment existing design methodologies. When implementing complex system architectures, these megafunctions significantly reduce design tasks, dramatically shorten design cycles, and leverage existing intellectual property (IP). By using megafunctions, designers can focus more time and energy on improving and differentiating their system-level product, rather than redesigning common off-the-shelf functions.

MegaCore Functions

MegaCore functions are pre-verified design files for complex system-level functions. These functions reduce the design task to creating only the custom logic surrounding these commonly used system-level functions, dramatically shortening the design cycle and leveraging existing intellectual property.

MegaCore functions are developed, pre-tested, documented, and licensed by Altera as MAX+PLUS® II add-on migration products. These functions are optimized for target Altera device architectures, including FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, and MAX 7000 devices, allowing the functions to be used without modification and ensuring that the function's optimization is preserved.

Altera provides all files necessary to design with MegaCore functions. Test vectors and a post-synthesis Altera Hardware Description Language (AHDL) design file, a fully minimized and optimized netlist that can be used without risk of changes during processing, are supplied for simulation in the MAX+PLUS II software. In addition, VHDL or Verilog HDL functional simulation models can be generated by the MAX+PLUS II software for verification with standard EDA simulation tools.

Using MegaCore Functions

MegaCore functions can be implemented into designs and simulated with the MAX+PLUS II development system or any Altera-supported EDA tool. For MAX+PLUS II design flows, the designer simply instantiates the function in the design file. For design flows that use third-party EDA tools, designers can instantiate MegaCore functions by specifying the function and port names in the HDL design file. Designers can then customize the function to meet design specifications by using a variety of parameters. During design processing, the EDA tool includes the function in an EDIF netlist file. The MAX+PLUS II software compiles the resulting EDIF netlist file for the desired Altera device architecture.

After using a MegaCore function in a design file, designers can use the MAX+PLUS II software to control how the design is compiled. For example, designers can perform the following tasks:

- Apply the WYSIWYG logic synthesis style to the function(s) in the design, ensuring that the MAX+PLUS II software will not further synthesize the function
- Specify timing performance requirements so that critical path requirements are met during design place-and-route

For more information on using the MAX+PLUS II development system, go to MAX+PLUS II Help.

MegaCore Offerings

Table 1 summarizes the MegaCore functions available from Altera.

Table 1. Altera MegaCore Functions (Part 1 of 2)

Product Name	Description	Target Device	Ordering Code
RGB2YCrCb and YCrCb2RGB	Color space converters	FLEX 10K FLEX 8000 FLEX 6000	PLSM-CSC
crc	Cyclic redundancy code generator and checker	FLEX 10K FLEX 8000 FLEX 6000	PLSM-CRC
fft	Fully parameterizable fast Fourier transform (FFT) function	FLEX 10K	PLSM-FFT
pci_a	Peripheral component interconnect (PCI) with direct memory access (DMA) controller	EPF10K20 EPF10K30	PLSM-PCI/A

Table 1. Altera MegaCore Functions (Part 2 of 2)

Product Name	Description	Target Device	Ordering Code
Microperipheral MegaCore Library	Library of universal asynchronous receiver/transmitter (UART), DMA controller, interrupt controller, and parallel port controller functions. Includes the a8237, a8251, a8255, a6402, a16450, a6850, and a8259 functions.	FLEX 10K FLEX 8000 FLEX 6000 MAX 9000 MAX 7000	PLSM-MICROLIB
a8237	Programmable DMA controller	FLEX 10K FLEX 8000 FLEX 6000	PLSM-8237
a8251	Programmable communications interface	FLEX 10K FLEX 8000 FLEX 6000	PLSM-8251
a8255	Programmable peripheral interface adapter	FLEX 10K FLEX 8000 FLEX 6000 MAX 9000 MAX 7000	PLSM-8255
a6402	Universal asynchronous receiver/transmitter	FLEX 10K FLEX 8000 FLEX 6000 MAX 9000 MAX 7000	PLSM-6402
a16450	Universal asynchronous receiver/transmitter	FLEX 10K FLEX 8000 FLEX 6000 MAX 9000 MAX 7000	PLSM-16450
a6850	Asynchronous communications interface adapter	FLEX 10K FLEX 8000 FLEX 6000 MAX 9000 MAX 7000	PLSM-6850
a8259	Programmable interrupt controller	FLEX 10K FLEX 8000 FLEX 6000 MAX 9000 MAX 7000	PLSM-8259

For more information on these MegaCore functions, refer to the following sources:

- *RGB2YCrCb & YCrCb2RGB Color Space Converters Data Sheet*
- *crc MegaCore Function Parameterized CRC Generator/Checker Data Sheet*
- *fft Fast Fourier Transform Data Sheet*
- *PCI Master/Target MegaCore Function with DMA Data Sheet*
- *Microperipheral MegaCore Function Data Book*

Altera Megafunction Partners Program

The Altera Megafunction Partners Program (AMPP), an alliance between Altera and developers of megafunctions, provides a wide variety of complex functions that are optimized for Altera devices. This alliance brings the advantages of additional sources of reusable designs to Altera PLD users while providing breadth to Altera's megafunction offering. Over 50 megafunctions are available from AMPP partners, including a Reed-Solomon coder / decoder (CODEC), an adaptable finite impulse response (FIR) filter, and 8- and 16-bit microprocessors.

AMPP megafunctions are intended as "drop-in" design elements for all design flows supported by the MAX+PLUS II development system. Although the megafunctions are developed as stand-alone functions, they can be integrated with other megafunctions and logic in a top-down design methodology.

AMPP megafunctions are available in VHDL, Verilog HDL, or post-synthesis AHDL format. These functions can be instantiated in a design file, including schematics and HDLs. AMPP partners optimize megafunctions to take advantage of the target device's architectural features, embedding the necessary place-and-route information to preserve performance and density during design processing.

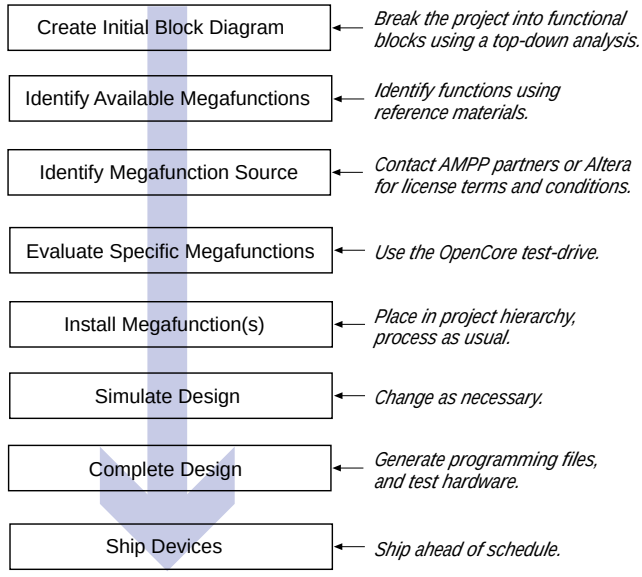
For more information on the AMPP program or a current listing of available AMPP megafunctions, refer to the *AMPP Catalog* or the Altera world-wide web (WWW) site at **http://www.altera.com**.

OpenCore Features

Designers can preview MegaCore and AMPP functions before purchase via the OpenCore™ feature. This pre-purchase evaluation system allows designers to instantiate, compile, and simulate a function to verify its size and performance. However, programming files as well as output files for third-party EDA tool simulation can be generated only with an authorization code provided when the megafunction is licensed.

Designers can download MegaCore functions for OpenCore evaluation from the Altera WWW site at **http://www.altera.com**; designers can obtain AMPP megafunctions for OpenCore evaluation directly from the AMPP partner. Figure 1 shows the typical design flow for evaluating megafunctions.

Figure 1. Design Flow for Evaluating Megafunctions



Conclusion

Altera MegaCore functions, in conjunction with AMPP megafunctions, provide designers with viable new options for implementing large, complex digital systems. These options are important for designers who want to use high-density PLDs, but who are faced with increasingly stringent time-to-market demands.